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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/757,643	01/13/2004	Mitsunori Sano	04016 /LH	3941

1933 7590 11/21/2005

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EXAMINER	
WILLIAMS, ALEXANDER O	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 11/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/757,643	SANO ET AL.	
	Examiner	Art Unit	
	Alexander O. Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *8-12 and 14-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/13/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Serial Number: 10/757643 Attorney's Docket #: 04016/LH
Filing Date: 1/13/2004; claimed foreign priority to 1/24/2003

Applicant: Sano et al.

Examiner: Alexander Williams

Applicant's election of the species of figures 2-4 (claims 1 to 7 and 13), filed 11/1/05, has been acknowledged.

This application contains claims 8 to 12 drawn to an invention non-elected without traverse.

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

The disclosure is objected to because of the following informalities: On page 5, line 9, "package resin 104" should probably be --anode terminal 104--.

Appropriate correction is required.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and

the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

Initially, and with respect to claims 1 and 13, note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Fitzgerald, 205 USPQ 594, 596 (CCPA); In re Marosi et al., 218 USPQ 289 (CAFC); and most recently, In re Thorpe et al., 227 USPQ 964 (CAFC, 1985) all of which make it clear that it is the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that Applicant has burden of proof in such cases as the above case law makes clear.

Claims 1 to 7 and 13, **insofar as they can be understood**, are rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicant's Prior Art existing Art figure 1 or Kayamori Takahiro (Japan Patent # 5-291079).

1. Applicant's Prior Art existing Art figure 1 show a chip type solid electrolytic capacitor comprising: a capacitor element **101**; a packaging resin **103** covering said capacitor element and having a mount surface **(bottom of the package 103)** and a side surface **(side of package 103)**

adjacent to said mount surface; and a terminal **107** electrically connected **(connected at the 104 and 102a)** to said capacitor element **101** and coupled to **(at 104 within 103)** said packaging resin, said terminal **107** extending along said mount surface and said side surface to have an outer surface **(outer surface of 107)** exposed from said packaging resin and to have an inner surface **(inner surface of 107)** opposite to said outer terminal surface, said inner surface having a stepwise shape formed by forging **(The Examiner is interested in finding the final structure claimed by Applicant. The process formed by is given little weight in examining device claims)**.

2. The chip type solid electrolytic capacitor according to claim 1, Applicant's Prior Art existing Art figure 1 show wherein said inner surface has a first step **(along the side of 107)** adjacent to said side surface and a second step **(along the side of the bottom of 107)** apart from said side surface, said first step being higher than said second step in a height from said mount surface.

3. The chip type solid electrolytic capacitor according to claim 2, Applicant's Prior Art existing Art figure 1 show wherein said capacitor element **101** has an anode lead **102a** extending towards said side surface, said terminal **107** being connected as an anode terminal **107** to said anode lead.

4. The chip type solid electrolytic capacitor according to claim 3, Applicant's Prior Art existing Art figure 1 show wherein said capacitor element **101** has a peripheral surface **101c**, said anode lead **102a** and said peripheral surface **101c** having a specific distance **(spaces between 101c and 102a)**

therebetween in said height, said first and said second steps having a particular distance greater than said specific distance.

5. The chip type solid electrolytic capacitor according to claim 2, Applicant's Prior Art existing Art figure 1 show wherein said capacitor element **101** has a cathode layer **106**, said terminal being connected as a cathode terminal **105,107** to said cathode layer **106**.

6. The chip type solid electrolytic capacitor according to claim 5, Applicant's Prior Art existing Art figure 1 show wherein said cathode terminal has a film formed on at least a part thereof, said film including at least one of Ag (silver), Au (gold), Cu (copper), and Pd (palladium).

7. The chip type solid electrolytic capacitor according to claim 5, Applicant's Prior Art existing Art figure 1 show wherein said cathode layer **106** is connected to said cathode terminal **105,107** by using conductive adhesive including Ag.

13. Applicant's Prior Art existing Art figure 1 show a chip type solid electrolytic capacitor comprising: a capacitor element **101** having an anode lead **102a** and a cathode layer **106**; a packaging resin **103** covering said capacitor element and having a mount surface **(bottom of the package 103)** and side surfaces **(side of package 103)** adjacent to said mount surface and opposite to each other; an anode terminal **104** electrically connected to said anode lead **102a** and coupled to said packaging resin **103**; and a cathode terminal **105,107** electrically connected to said cathode layer **106** and coupled to said packaging resin **103**, each of said anode terminal **104,107** and said cathode terminal **105,107** extending along said mount surface and each of said side surfaces to have an outer surface

exposed from said packaging resin and to have an inner surface apposite to said outer surface, said inner surface having a stepwise shape formed by forging **(The Examiner is interested in finding the final structure claimed by Applicant. The process formed by is given little weight in examining device claims)**.

As to the grounds of rejection under section 103, see MPEP § 2113.

Claims 1 to 7 and 13, **insofar as they can be understood**, are rejected under 35 U.S.C. § 103(a) as being unpatentable over Kanetake (U.S. Patent Application Publication # 2004/0103508 A1).

1. Kanetake (figures 1 to 14) specifically figure 1 show a chip type solid electrolytic capacitor comprising: a capacitor element **10**; a packaging resin **3** covering said capacitor element and having a mount surface **(30 bottom of the package 3)** and a side surface **(side of package 3)** adjacent to said mount surface; and a terminal **21** electrically connected **(connected at the 11b)** to said capacitor element **10** and coupled to **(at 11b)** said packaging resin, said terminal **21** extending along said mount surface and said side surface to have an outer surface **(outer surface of 21b)** exposed from said packaging resin and to have an inner surface **(inner surface of 21b)** opposite to said outer terminal surface, said inner surface having a stepwise shape formed by forging **(The Examiner is interested in finding the final structure claimed by Applicant. The process formed by is given little weight in examining device claims)**.

2. The chip type solid electrolytic capacitor according to claim 1, Kanetake show wherein said inner surface has a first step **(along the side of 21)**

adjacent to said side surface and a second step **(along the side of the bottom of 21)** apart from said side surface, said first step being higher than said second step in a height from said mount surface.

3. The chip type solid electrolytic capacitor according to claim 2, Kanetake show wherein said capacitor element **10** has an anode lead **11** extending towards said side surface, said terminal **21** being connected as an anode terminal **11** to said anode lead.

4. The chip type solid electrolytic capacitor according to claim 3, Kanetake show wherein said capacitor element **10** has a peripheral surface **12**, said anode lead **11** and said peripheral surface **12** having a specific distance **(spaces between them)** therebetween in said height, said first and said second steps having a particular distance greater than said specific distance.

5. The chip type solid electrolytic capacitor according to claim 2, Kanetake show wherein said capacitor element **10** has a cathode layer **40**, said terminal being connected as a cathode terminal **20** to said cathode layer **40**.

6. The chip type solid electrolytic capacitor according to claim 5, Kanetake show wherein said cathode terminal **20** has a film formed on at least a part thereof, said film including at least one of Ag (silver), Au (gold), Cu (copper), and Pd (palladium).

7. The chip type solid electrolytic capacitor according to claim 5, Kanetake show wherein said cathode layer **40** is connected to said cathode terminal **20** by using conductive adhesive including Ag.

13. Kanetake (figures 1 to 14) specifically figure 1 show a chip type solid electrolytic capacitor comprising: a capacitor element **10** having an anode lead **11** and a cathode layer **40**; a packaging resin **3** covering said capacitor element and having a mount surface **(30 bottom of the package 3)** and side surfaces **(side of package 3)** adjacent to said mount surface and opposite to each other; an anode terminal **21** electrically connected to said anode lead **11** and coupled to said packaging resin **3**; and a cathode terminal **20** electrically connected to said cathode layer **40** and coupled to said packaging resin **3**, each of said anode terminal **21** and said cathode terminal **20** extending along said mount surface and each of said side surfaces to have an outer surface exposed from said packaging resin and to have an inner surface apposite to said outer surface, said inner surface having a stepwise shape formed by forging **(The Examiner is interested in finding the final structure claimed by Applicant. The process formed by is given little weight in examining device claims)**.

As to the grounds of rejection under section 103, see MPEP § 2113.

Claims 1 to 7 and 13, **insofar as they can be understood**, are rejected under 35 U.S.C. § 103(a) as being unpatentable over Kuriyama (U.S. Patent # 6,819,546 B2).

1. Kuriyama (figures 1 to 156) specifically figure 74 show a chip type solid electrolytic capacitor comprising: a capacitor element **6**; a packaging resin **17** covering said capacitor element and having a mount surface **(bottom of the package 17,11)** and a side surface **(side of package 17a)** adjacent to said mount surface; and a terminal **18,14** electrically connected **(connected by 6b)** to said capacitor element **6** and coupled to said

packaging resin, said terminal **18** extending along said mount surface and said side surface to have an outer surface **(outer surface of 18)** exposed from said packaging resin and to have an inner surface **(inner surface of 18)** opposite to said outer terminal surface, said inner surface having a stepwise shape formed by forging **(The Examiner is interested in finding the final structure claimed by Applicant. The process formed by is given little weight in examining device claims)**.

2. The chip type solid electrolytic capacitor according to claim 1, Kuriyama show wherein said inner surface has a first step **(along the side of 18)** adjacent to said side surface and a second step **(along the side of the bottom of 18)** apart from said side surface, said first step being higher than said second step in a height from said mount surface.

3. The chip type solid electrolytic capacitor according to claim 2, Kuriyama show wherein said capacitor element **6** has an anode lead **6b** extending towards said side surface, said terminal **18** being connected as an anode terminal **18** to said anode lead.

4. The chip type solid electrolytic capacitor according to claim 3, Kuriyama show wherein said capacitor element **6** has a peripheral surface, said anode lead **6b** and said peripheral surface having a specific distance **(spaces between them)** therebetween in said height, said first and said second steps having a particular distance greater than said specific distance.

5. The chip type solid electrolytic capacitor according to claim 2, Kuriyama show wherein said capacitor element **6** has a cathode layer **6d**, said

terminal being connected as a cathode terminal **19,13** to said cathode layer **6d**.

6. The chip type solid electrolytic capacitor according to claim 5, Kuriyama show wherein said cathode terminal **19,13** has a film formed on at least a part thereof, said film including at least one of Ag (silver), Au (gold), Cu (copper), and Pd (palladium).

7. The chip type solid electrolytic capacitor according to claim 5, Kanetake show wherein said cathode layer **6d** is connected to said cathode terminal **19,13** by using conductive adhesive including Ag.

13. Kuriyama (figures 1 to 156) specifically figure 74 show a chip type solid electrolytic capacitor comprising: a capacitor element **6** having an anode lead **6b** and a cathode layer **6d**; a packaging resin **17** covering said capacitor element and having a mount surface **(bottom of the package 17)** and side surfaces **(side of package 17a)** adjacent to said mount surface and opposite to each other; an anode terminal **18,14** electrically connected to said anode lead **6b** and coupled to said packaging resin **17**; and a cathode terminal **19,13** electrically connected to said cathode layer **6d** and coupled to said packaging resin **17**, each of said anode terminal **18,14** and said cathode terminal **20** extending along said mount surface and each of said side surfaces to have an outer surface exposed from said packaging resin and to have an inner surface apposite to said outer surface, said inner surface having a stepwise shape formed by forging **(The Examiner is interested in finding the final structure claimed by Applicant. The process formed by is given little weight in examining device claims)**.

As to the grounds of rejection under section 103, see MPEP § 2113.

The listed references are cited as of interest to this application, but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/528,532,728,666,696,698,684,796,773,783,535 361/528,529,534,433,310,535,538,540,538 29/25.42,592.1,25.03,832,417,301.1	11/16/05
Other Documentation: foreign patents and literature in 257/528,532,728,666,696,698,684,796,773,783,535 361/528,529,534,433,310,535,538,540,538 29/25.42,592.1,25.03,832,417,301.1	11/16/05
Electronic data base(s): U.S. Patents EAST	11/16/05

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O. Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30AM-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Alexander O Williams
Primary Examiner
Art Unit 2826

AOW
11/16/05